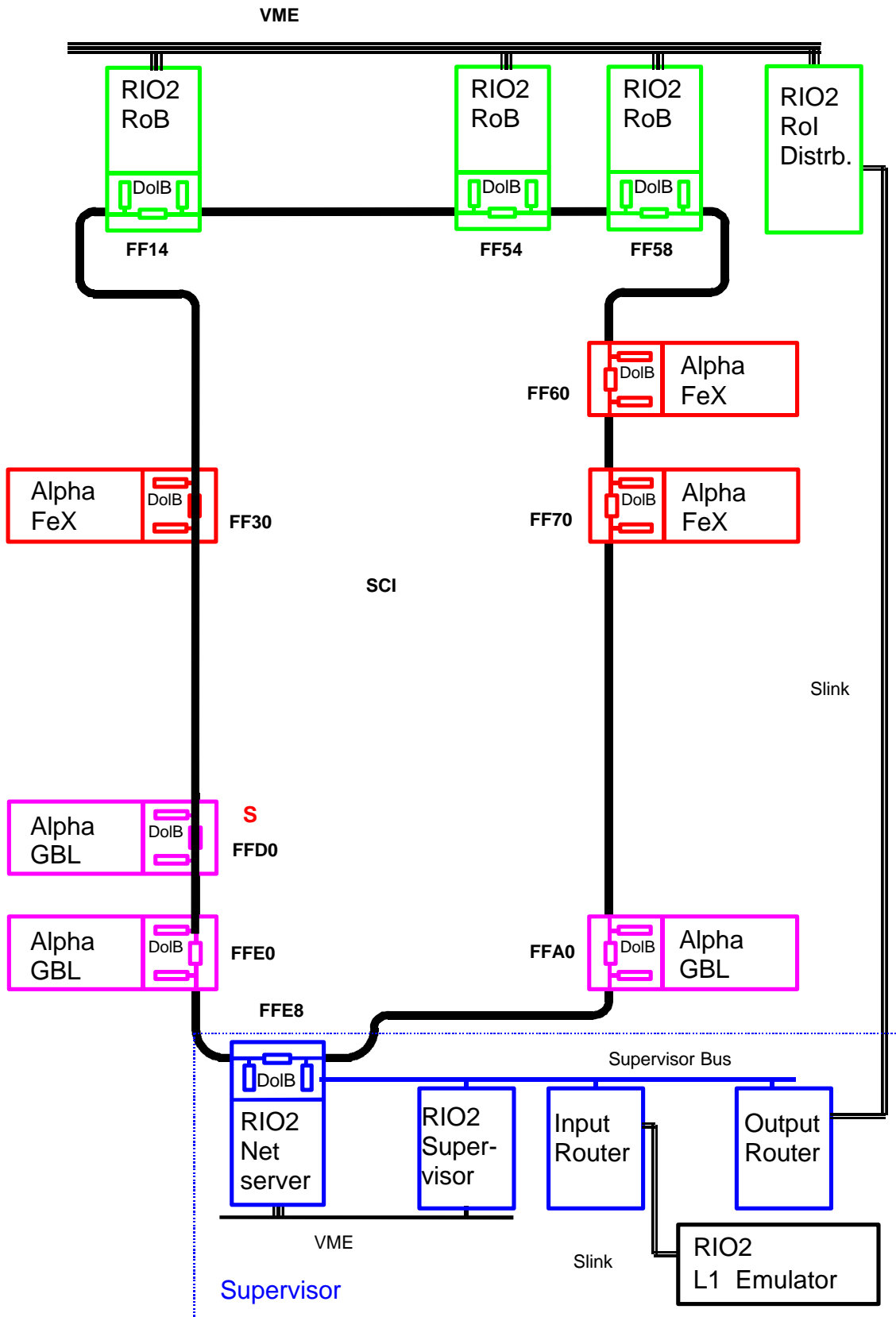
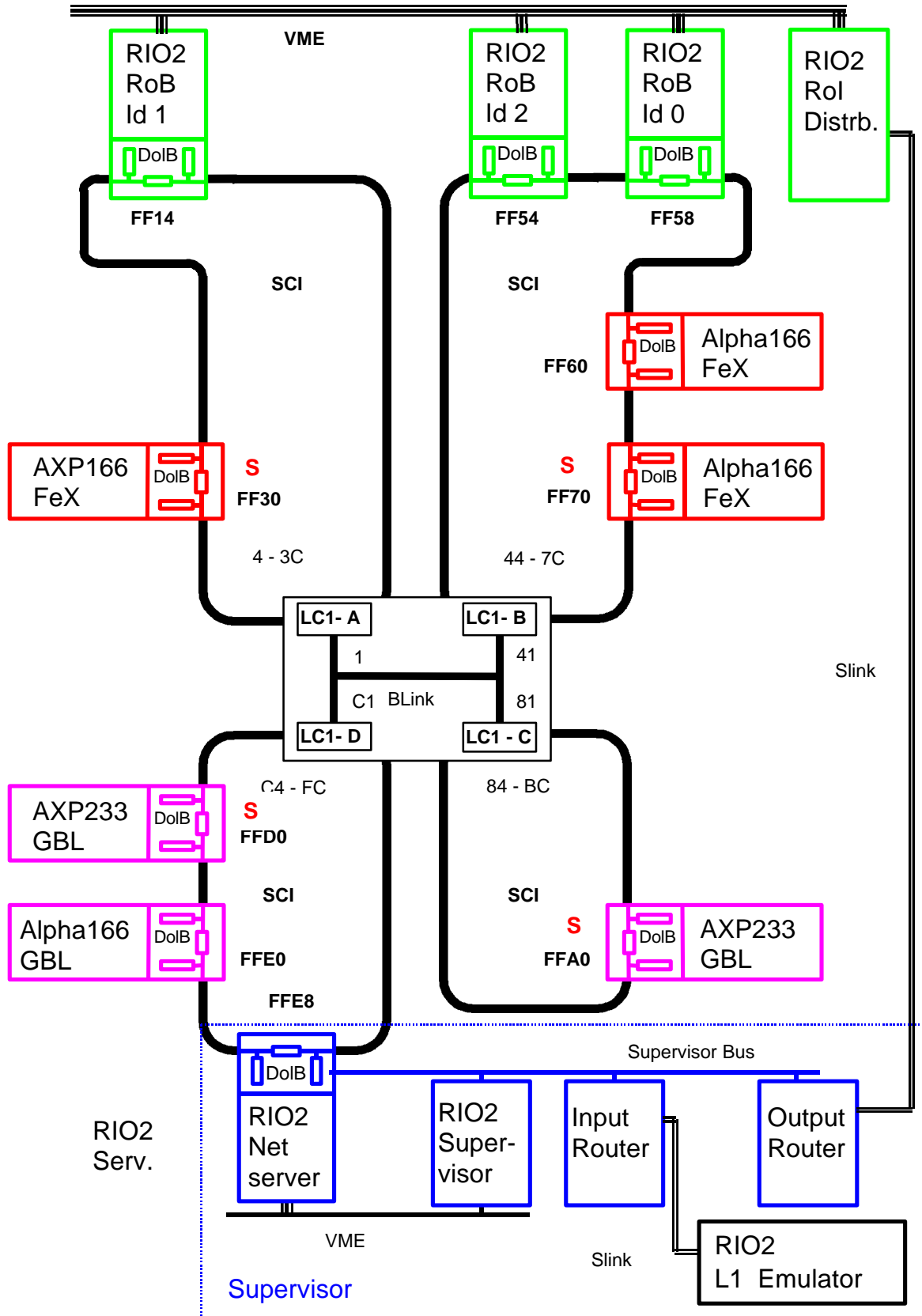


SCI Ring Connecting 3 RoB, 3 FeX, 3 Global & the Supervisor

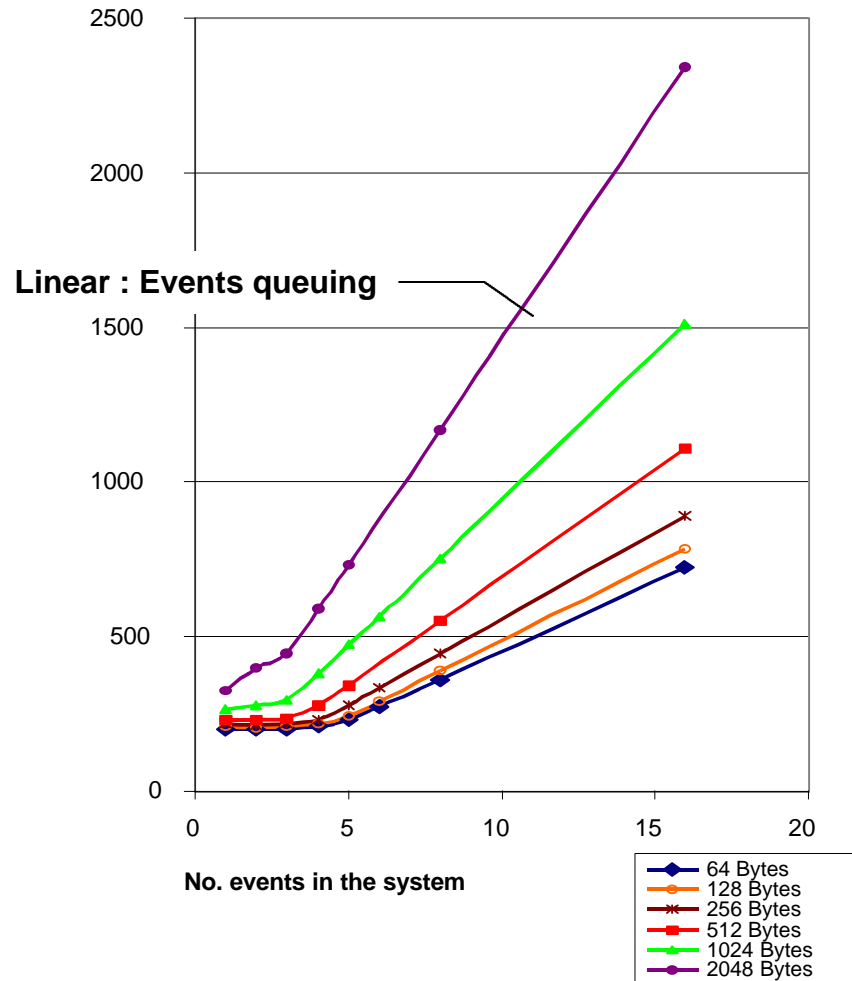


SCI Ring with a 4*4 Switch Connecting 3 RoB, 3 FeX, 3 Global & the Supervisor

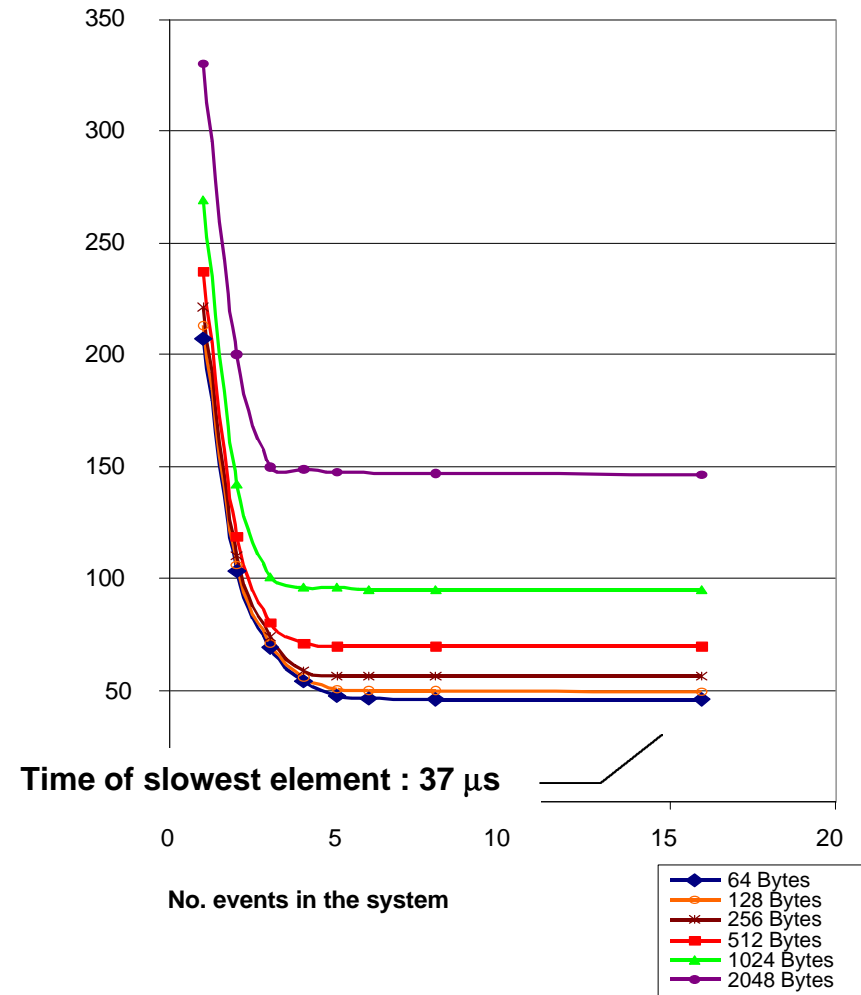


Results: 1RoI/event through 1 Stripe of 1 RoB 1 FeX 1 Global

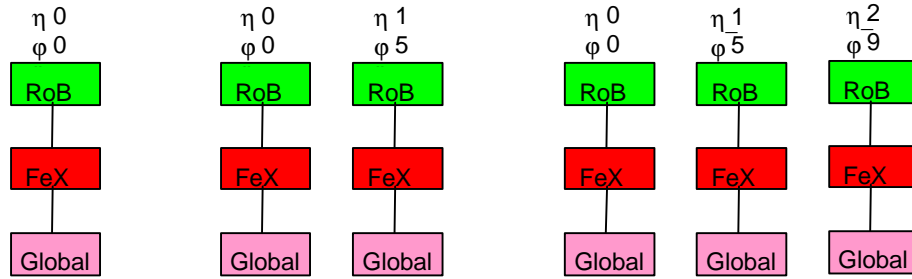
Latency vs no. events in system
1RoI/event 1RoB 1FeX 1Global



Ave. time / event vs no. events
1RoI/event 1RoB 1FeX 1Global



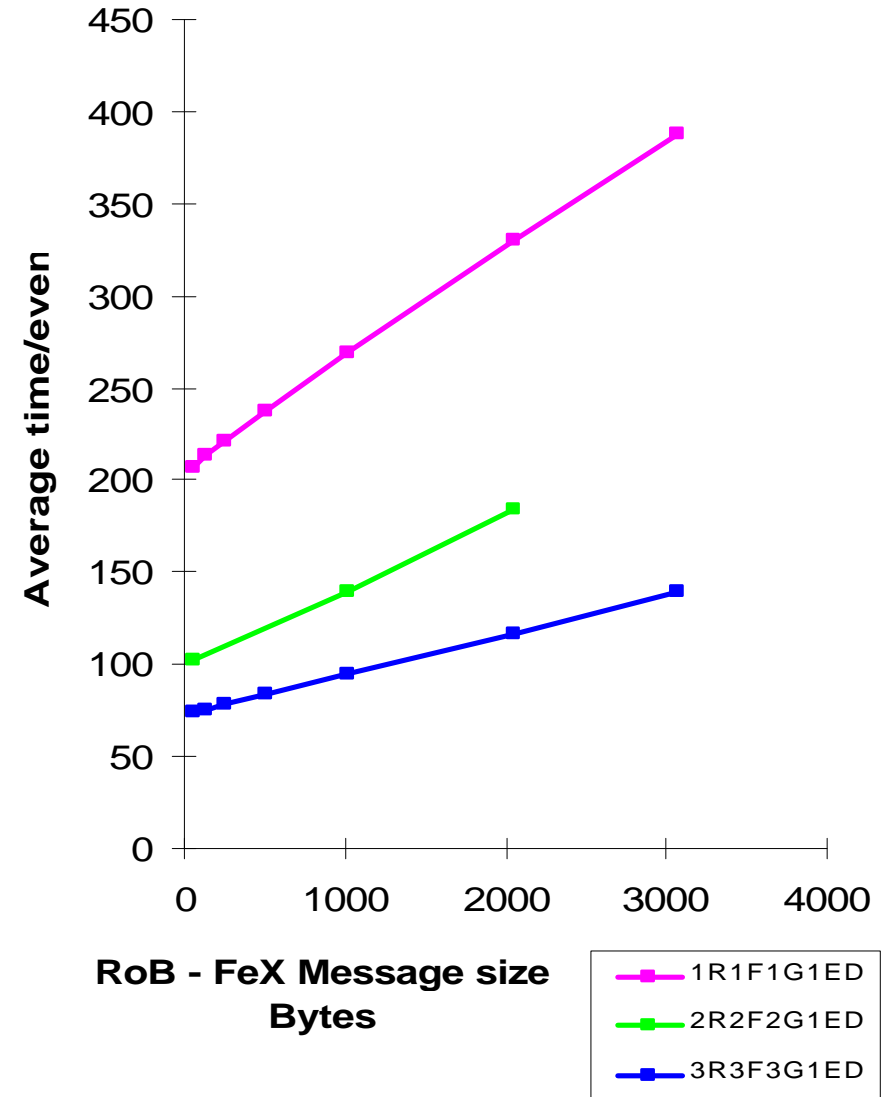
Results: Events in Parallel RoB-FeX-Global Stripes



The ratios of average times scale:

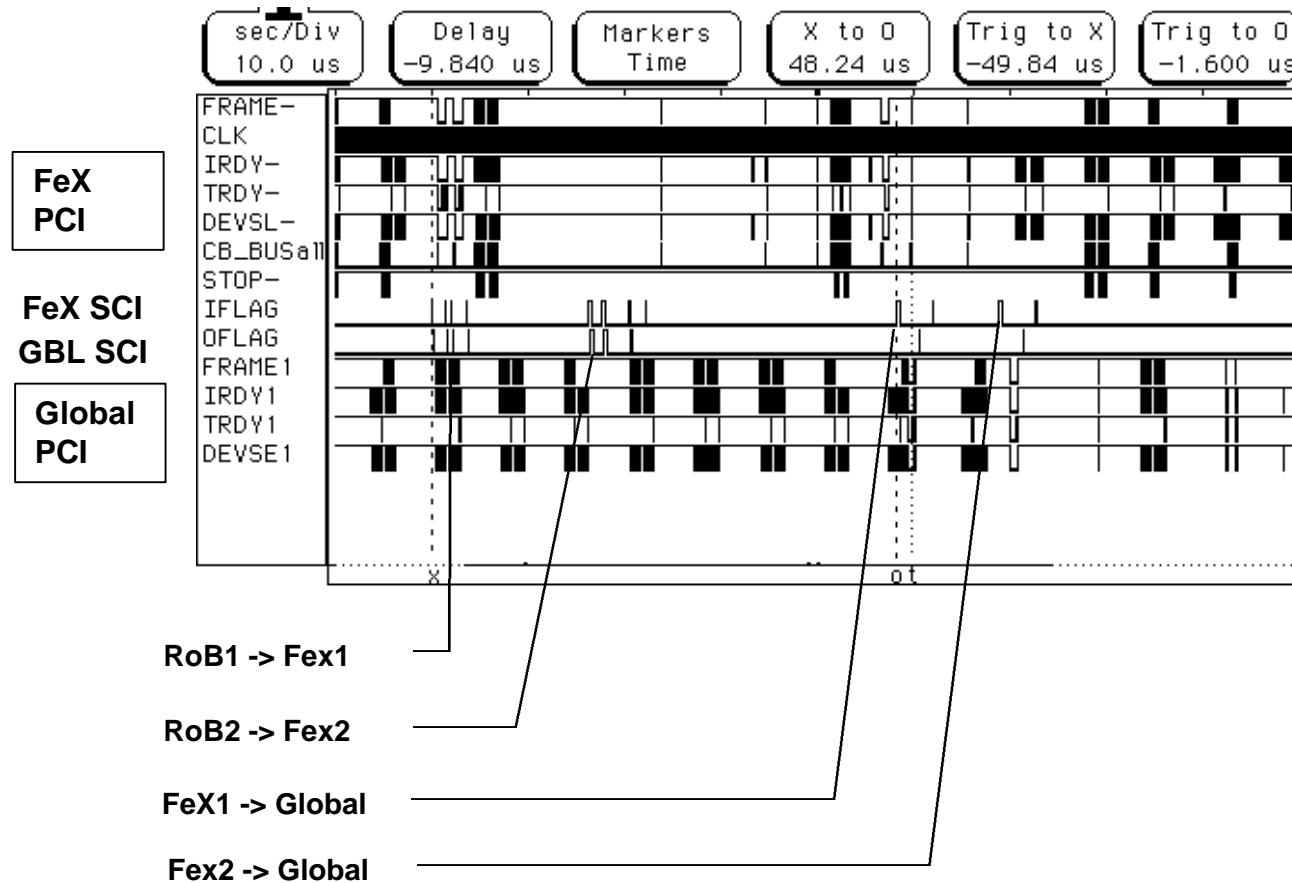
	64 Bytes	1024 Bytes
1R1F1GD	1.0	1.0
2R2F2GD	2.03	1.9
3R3F3GD	2.8	2.8

- Supervisor & RoI Distributor shared.
- SCI Transfers not concurrent as expected



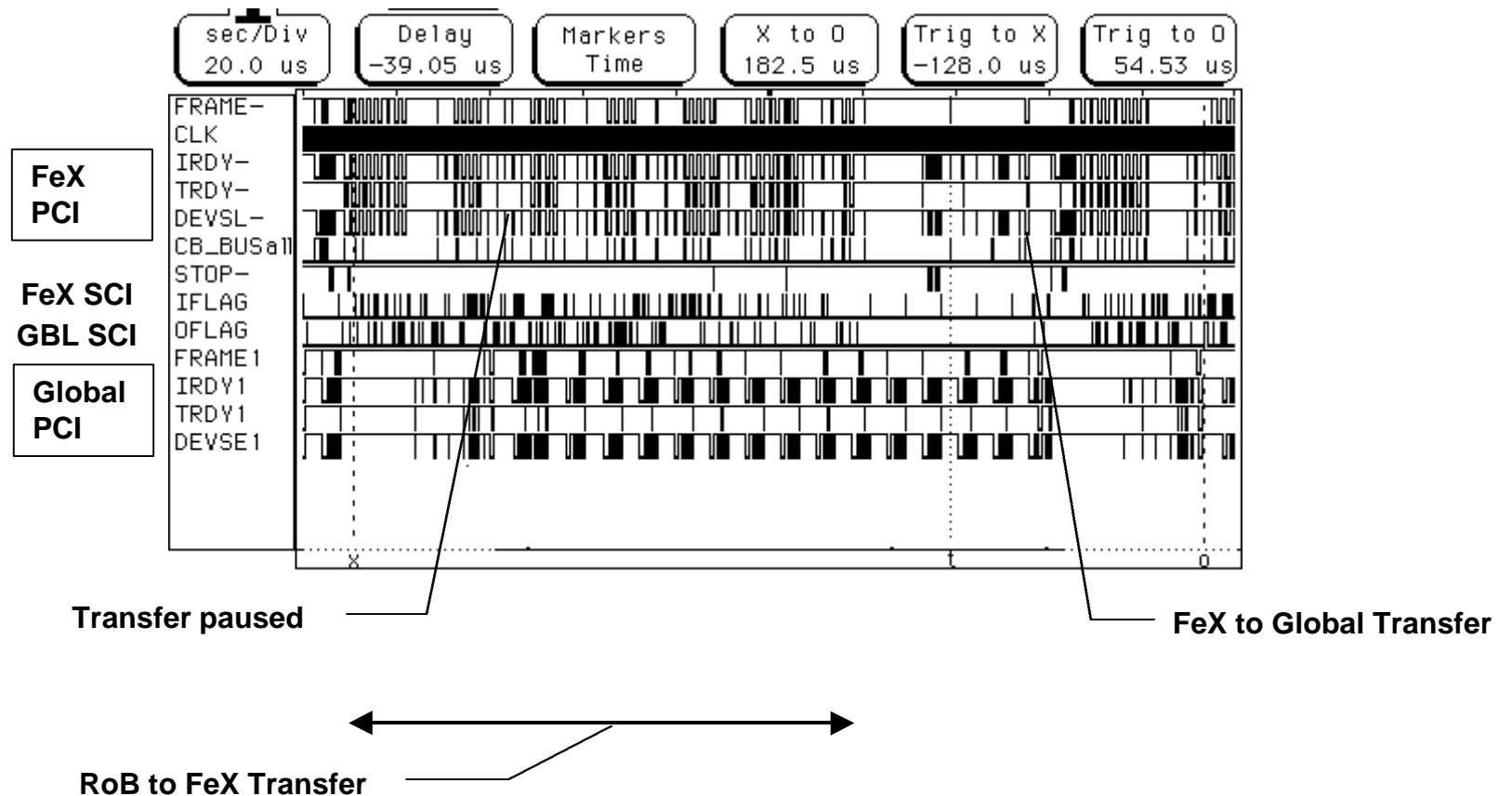
Probing PCI & SCI : RoB to FeX Times for Multiple Events

Time between RoB1 and RoB2 outputs of 16.4 μ s due to the RoI Distributor sequence time

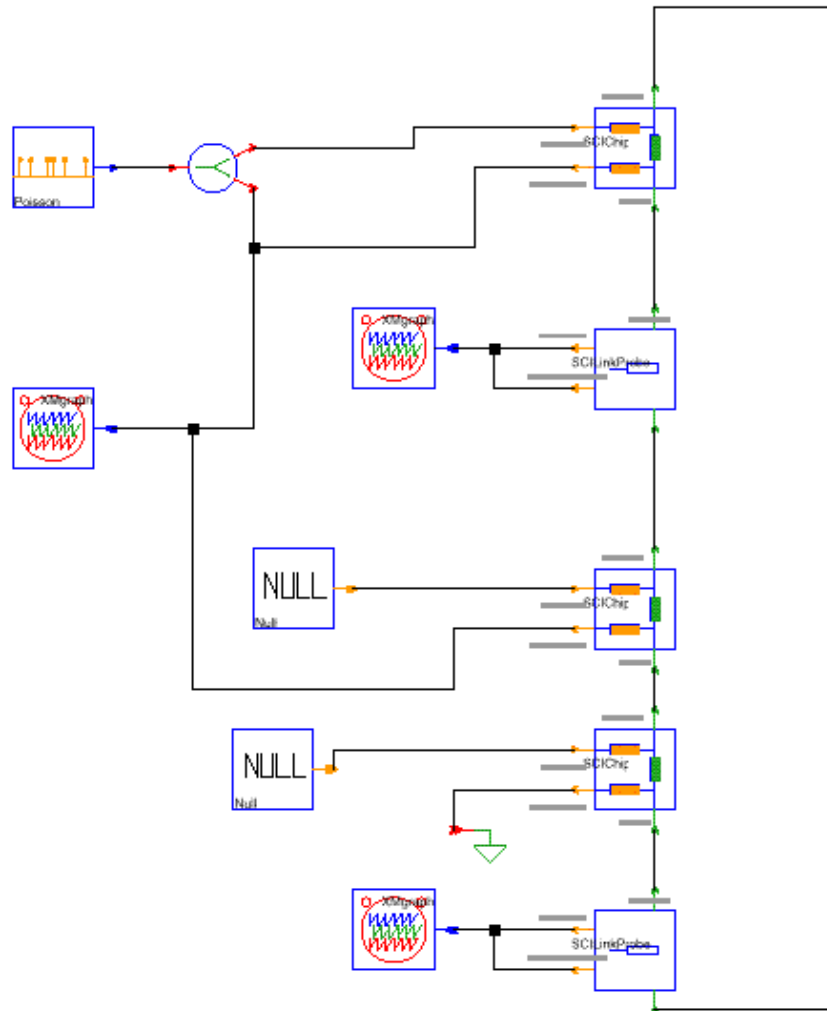


Probing PCI & SCI : 2 RoBs to FeX Transfers with 4 Events

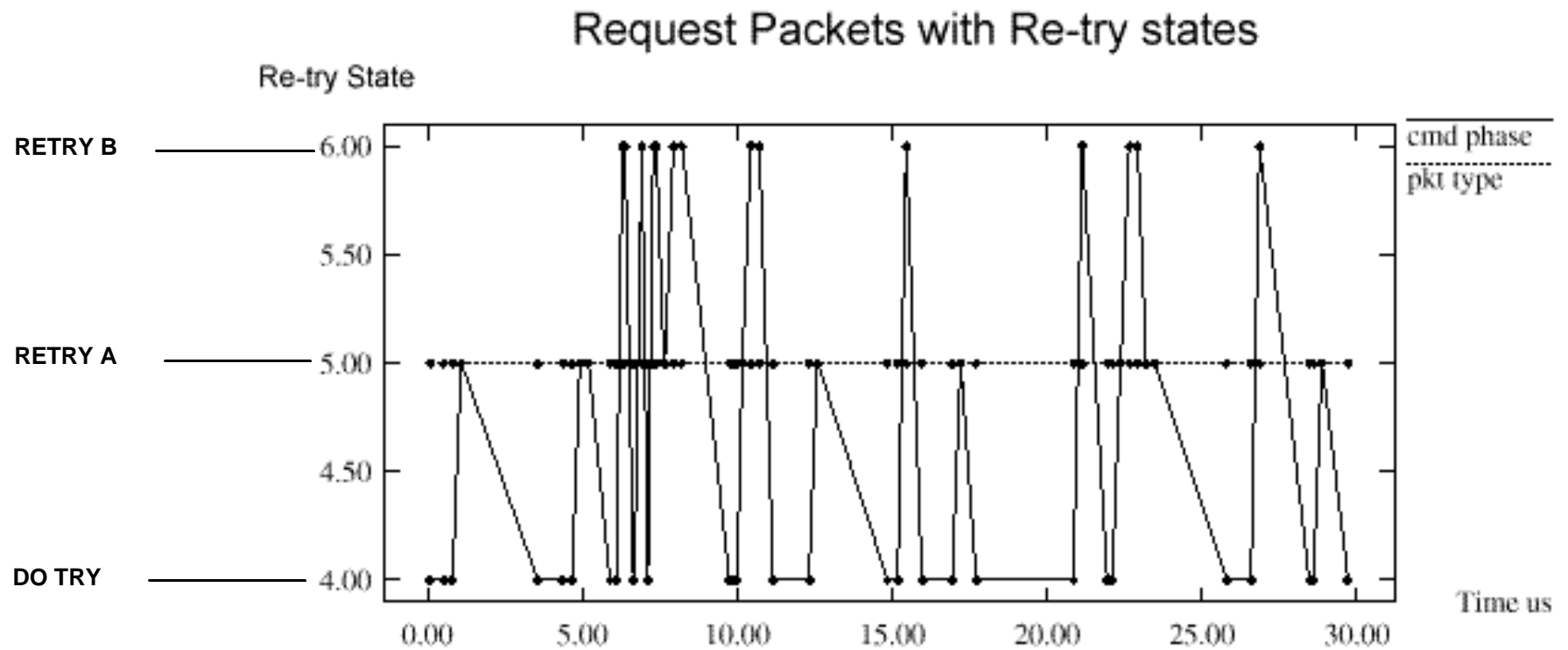
DMA transfers between the RoBs and the FeX paused for ~10 μ s due to sharing of the PCI bus in the RoB



Ptolemy Simulation of a SCI Ringlet



Ptolemy : Simulation of SCI Re-Tries



Ptolemy Simulation of a Gigabit Ethernet Link

